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[Title Of The Invention]
REPAIR STRUCTURE AND REPAIR METHOD OF I/O PIN

[Abstract]
PURPOSE: To provide a repair structure and a repair method of restoring a damaged I/O pin so as to have an original electrical and mechanical characteristic in the case where the external connecting I/O pin provided on a ceramic multi-layer wiring board comes off together with a part of the ceramic board and damaged.
CONSTITUTION: Conductive adhesive 7 is embedded in a damaged part of an I/O pin, and a repair pin 6 is errected, made to adhere thereto, and electrically connected to the damaged part, and a normal I/O pin 5 and a repair pin 6 surrounding the damaged I/O pin are bridged and fixed to a fixing plate 8 to obtain mechanical strength.

[Claim(s)]
[Claim 1]Repair structure of an I/O pin constructing a bridge and fixing an I/O pin which newly adhered to an I/O pin breakage part on multilayer interconnection boards, such as ceramics, and a normal I/O pin located in the circumference of this I/O pin by a stationary plate.
[Claim 2]Repair structure of the I/O pin according to claim 1 using electroconductive glue for a breakage part of an I/O pin on multilayer interconnection boards, such as ceramics, and adhering a new I/O pin.
[Claim 3]A repair method of an I/O pin including the 2nd process of constructing a bridge and fixing the 1st process of adhering a new I/O pin to an I/O pin breakage part on multilayer interconnection boards, such as ceramics, and said new I/O pin and a normal I/O pin located in the circumference by a stationary plate.

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the repair structure and the repair method of an I/O pin which were formed in multilayer interconnection boards, such as ceramics.
[0002]
[Description of the Prior Art]Conventionally, as multilayer interconnection boards, such as ceramics in which the I/O pin was formed, there is a pin grid array of a single chip module.
[0003]In such a multilayer interconnection board, the LSI chip is mounted in the surface of substrates, such as ceramics, and two or more I/O pins electrically connected with the LSI chip via two or more through holes formed in the substrate are formed in the rear face.
[0004]If it is in the multilayer interconnection board like the above, since the I/O pin is thin, it may damage, as shown in drawing 9 thru/or drawing 12.
[0005]That is, drawing 9 shows the case where the I/O pin 51 damages by a shaft part, and drawing 10 shows the case where the I/O pin 51 is damaged in a brazing portion. Both drawing 11 shows the case where the I/O pin 51 and the mounting pad 52 exfoliated from

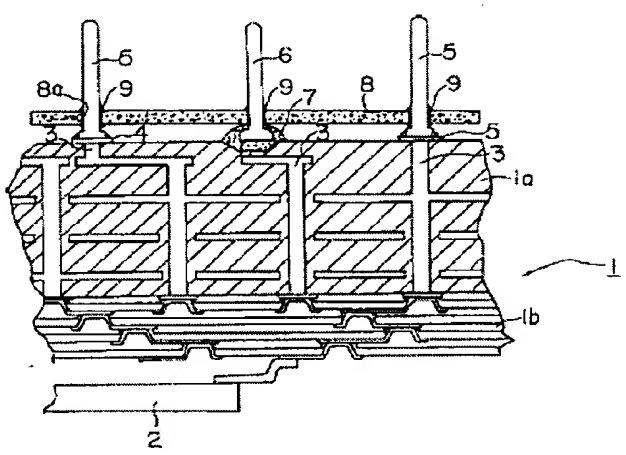
the ceramic substrate 53, and are damaged, and drawing 12 shows the case where the ceramic substrate 53 is also damaged with the I/O pin 51.
[0006]
[Problem(s) to be Solved by the Invention]In the conventional multilayer interconnection board, even if the I/O pin was damaged, repair of the damaged I/O pin is not performed and the multilayer interconnection board itself was exchanged.
[0007]For this reason, there was a problem that repair cost became high, in the electronic device using the high substrate of added value like a single chip module.
[0008]the purpose of this invention -- the I/O pin on multilayer interconnection boards, such as ceramics, -- a mounting pad -- or it is in providing the repair structure and the repair method at the time of damaging with a part of ceramic substrate.
[0009]
[Means for Solving the Problem]Repair structure of multilayer substrates, such as ceramics of this invention, has a stationary plate which constructs a bridge in an I/O pin which newly adhered to an I/O pin breakage part, and an I/O pin located in the circumference of this I/O pin.
[0010]
[Example]Next, this invention is explained with reference to drawings.
[0011]The sectional view and drawing 2 which drawing 1 shows the repair structure of one example of this invention are a sectional view showing a normal multilayer interconnection board.
[0012]In advance of explanation of the repair structure of this invention, and a repair method, the composition of the multilayer interconnection board in the state where the I/O pin is not damaged by drawing 2 is explained.
[0013]The multilayer interconnection board 1 is constituted in drawing 2 by the fine wiring layer 1b which makes layer insulation the polyimide formed in the surface of the ceramic substrate 1a and this ceramic substrate 1a. LSI chip 2 is mounted in the upper surface of the fine wiring layer 1b.
[0014]Two or more through holes 3 are formed in the ceramic substrate 1a, it is a rear face of the ceramic substrate 1a, and the mounting pad 4 is formed corresponding to each through hole 3. And the I/O pin 5 for external connection is soldered by each mounting pad 4, and it is electrically connected with LSI chip 2 via the through hole 3 of the ceramic substrate 1a.
[0015]The diameter of the through hole 3 is set as 0.25 mm, and conductive paste, such as tungsten, molybdenum, gold, silver, and silver-palladium, is embedded inside. The diameter of the mounting pad 4 is set as 1.3 mm, and is formed with sputter films, such as a gold plating film, a coppering film, thick film gold, thick film copper, or palladium.
[0016]The I/O pin 5 has 0.35 mm in diameter, and a size 5.0 mm in length, and is formed. In order for the end face joined to the mounting pad 5 of the I/O pin 5 to increase adhesion area and to obtain sufficient intensity, header working is performed, and gold plate is performed to the surface. Generally as wax material for soldering the I/O pin 5 to the mounting pad 4, the wax material of eutectic alloys, such as gold / tin:80/20 (wt%) or silver / copper:72/28 (wt%), is used.
[0017]the I/O pin of the center in the inside of two or more I/O pins 5 by which drawing 1 was provided in the rear face of the ceramic substrate 1a, and a figure -- a mounting pad -- or the repair structure at the time of damaging with a part of ceramic substrate 1a is shown.

[0018]The I/O pin (repair pin) 6 new in the position of the damaged I/O pin has adhered to the ceramic substrate 1a with the electroconductive glue 7. The repair pin 6 is supported by a bridge being constructed by the normal I/O pin 5 and the stationary plate 8 in the circumference of this repair pin 6, and fixing each I/O pin 5 and 6 to the stationary plate 8 with the adhesives 9.
[0019]Such a repair structure and a repair method are concretely explained using drawing 3 - drawing 5.
[0020]First, the electroconductive glue 7 is embedded in the position of the I/O pin damaged as shown in drawing 3, and this electroconductive glue 7 is made to carry out standing-up adhesion of the repair pin 6. At this time, the position which raises the repair pin 6 measures and deduces the size from the normal I/O pin 5 in the circumference. As the electroconductive glue 7 for pasting up the repair pin 6, what consists of golden-polyimide, silver-epoxy, etc. is used. Thus, it is possible to fix the multilayer interconnection board 1 by pasting up the repair pin 6 on the breakage position of an I/O pin with the electroconductive glue 7.
[0021]However, it is difficult to adhere this repair pin 6 to the ceramic substrate 1a firmly only by pasting up the repair pin 6 on the ceramic substrate 1a with the electroconductive glue 7.
[0022]For this reason, as shown in the perspective view of drawing 4, a bridge is constructed by the stationary plate 8 in the I/O pin 5 joined to the ceramic substrate 1a in the normal state of being in the circumference of the repair pin 6 and this repair pin 6, And by pasting up the I/O pin 5 and the repair pin 6 on the stationary plate 8 with the adhesives 9, the repair pin 6 is supported by the surrounding I/O pin 5 via the stationary plate 8.
[0023]In this example, the 0.635-mm-thick ceramic plate is used as the stationary plate 8, and the nine holes 8a 0.4 mm in diameter are formed in the pitch equal to the pitch of the I/O pin 5 to this stationary plate 8. Although the path of the hole 8a is prescribed by the accuracy of position at the time of raising the repair pin 6, it is preferred that it is a value larger about 0.1 mm than the diameter of the I/O pin 5 and the repair pin 6.
[0024]It is possible to use the thing of an epoxy system or a ceramic system as the adhesives 9, and it is preferred to be filled up with these adhesives 9 between each pins 5 and 6 and the hole 8a.
[0025]Drawing 5 is drawing of longitudinal section in the A-A line of drawing 4. As shown in a figure, it fills up with adhesives between the hole 8a, the I/O pin 5, and the repair pin 6 which were formed in the stationary plate 8, and the stationary plate 8 is allocated by the root of each pins 5 and 6. Thus, it is possible to guarantee the intensity of the pins 5 and 6, such as this, by allocating the stationary plate 8 in the root of each pins 5 and 6.
[0026]Drawing 6 fills up the whole header of the I/O pin 5 and the repair pin 6 with the adhesives 9, and pastes up with the stationary plate 8.
[0027]In this case, it is preferred to choose the adhesives 9 excellent in migration resistance nature so that the migration of each pin 5 which adjoins inside the adhesives 9, and 6 may not occur.
[0028]Drawing 7 forms the nine holes 10a in a pitch equal to the pitch of the I/O pin 5 and the repair pin 6, and it is a sectional view of repair structure using the stationary plate 10 which formed the crevice 10b in the position corresponding to the header of the pins 5 and 6.

[0029]The construction material of the stationary plate 10, thickness, etc. are the same as that of the stationary plate 8 in the above-mentioned example.
[0030]In this case, it becomes it is possible to make the rear face of the ceramic substrate 1a carry out abbreviated direct contact of the solid plate 10, and possible to lengthen the wire extension from the stationary plate 10 of each pins 5 and 6.
[0031]Drawing 8 forms the nine holes 11a in a pitch equal to the pitch of the I/O pin 5 and the repair pin 6, and it is a sectional view of repair structure using the stationary plate 11 which formed the boss-like projection 11b in the circumference of the hole 11a.
[0032]The construction material of the stationary plate 11 and thickness are the same as that of the stationary plates 8 and 10 in each above-mentioned example.
[0033]In this case, it becomes it is possible to lengthen the contact length of the stationary plate 11 and each pins 5 and 6, and possible to fix the repair pin 6 more firmly.
[0034]Although the ceramic plate was used as the stationary plates 8, 10, and 11 in each above-mentioned example, it is possible to use, if it does not limit to this construction material and being excelled in electrical insulation, intensity, and heat resistance. The number of the holes 8a, 10a, and 11a formed in the stationary plates 8, 10, and 11 is not limited to nine pieces, and what is necessary is just to choose it within limits which can maintain the intensity of the repair pin 6.
[0035]
[Effect of the Invention]As explained above, this invention can fix this multilayer interconnection board, even if this breakage is a serious thing which omits a part of ceramic substrate, when the I/O pin for the external connection of multilayer interconnection boards, such as ceramics, is damaged. For this reason, it has the effect that an electronic device can be fixed without exchanging an expensive multilayer substrate.
[Brief Description of the Drawings]
[Drawing 1]It is a sectional view showing the repair structure of the multilayer interconnection board of one example of this invention.
[Drawing 2]It is a sectional view of a normal multilayer interconnection board.
[Drawing 3]It is a sectional view which illustrates like the repair man of a multilayer interconnection board.
[Drawing 4]It is a perspective view which illustrates like the repair man of a multilayer interconnection board.
[Drawing 5]It is a sectional view which illustrates like the repair man of a multilayer interconnection board.
[Drawing 6]It is a sectional view explaining other repair structures of a multilayer interconnection board.
[Drawing 7]It is a sectional view explaining other repair structures of a multilayer interconnection board.
[Drawing 8]It is a sectional view explaining other repair structures of a multilayer interconnection board.
[Drawing 9]It is a sectional view explaining the breakage state of an I/O pin.
[Drawing 10]It is a side view explaining the breakage state of an I/O pin.
[Drawing 11]It is a side view explaining the breakage state of an I/O pin.
[Drawing 12]It is a side view explaining the breakage state of an I/O pin.
[Description of Notations]
1 Multilayer interconnection board

1a Ceramic substrate
1b Fine wiring layer
2 LSI chip
3 Through hole
4 Mounting pad
5 I/O pin
6 Repair pin
7 Electroconductive glue
8, 10, and 11 Stationary plate
8a, 10a, and 11a Hole
9 Adhesives
11b Crevice
12 Projection

【図１】



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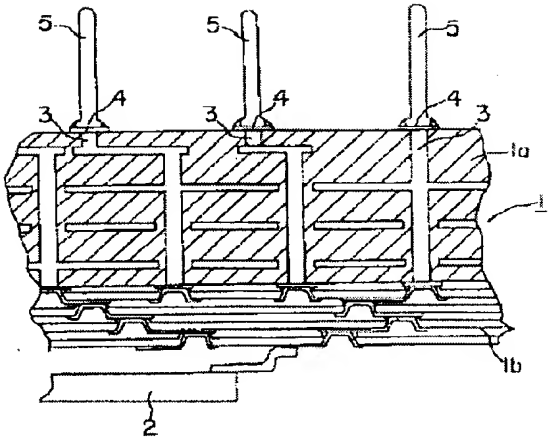

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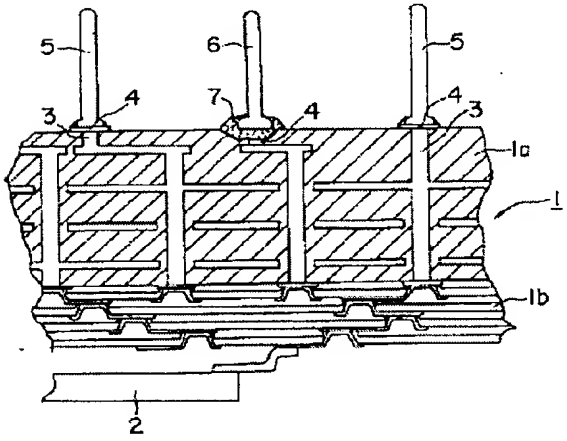

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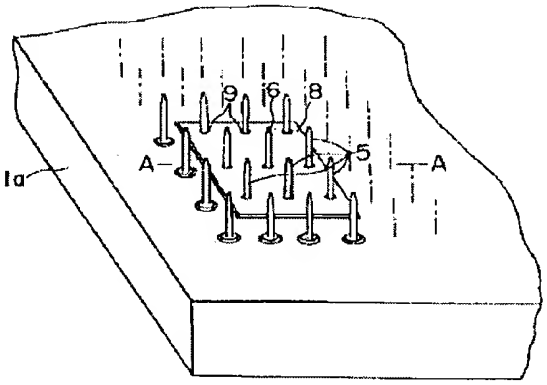

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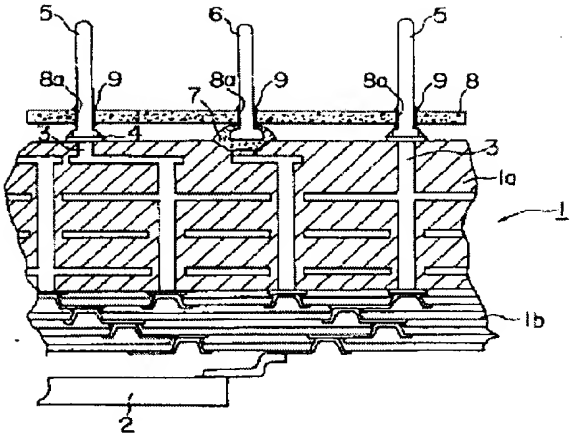

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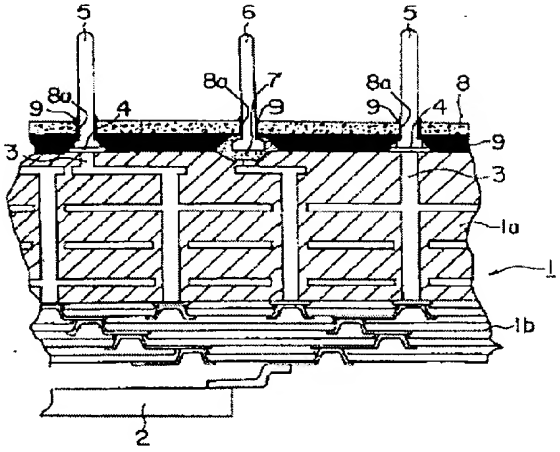

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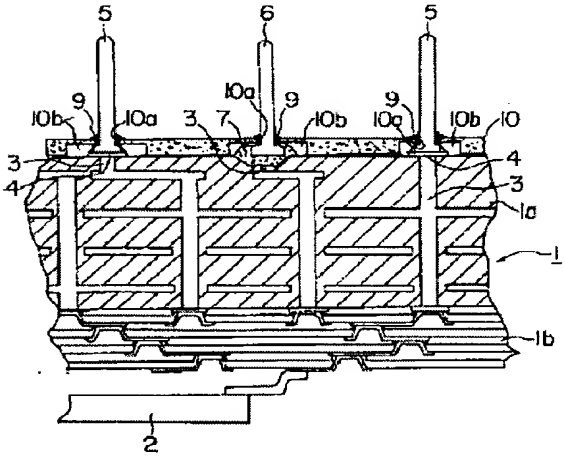

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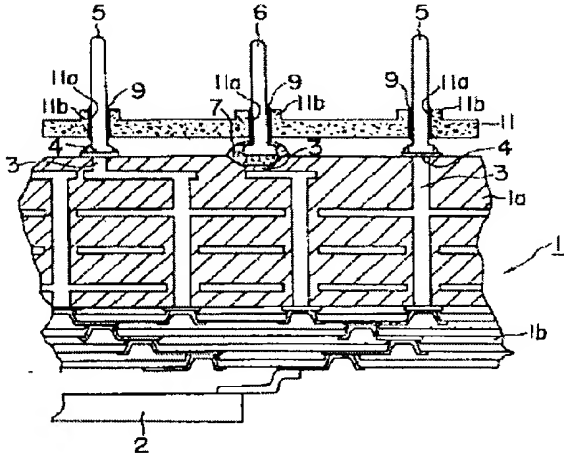

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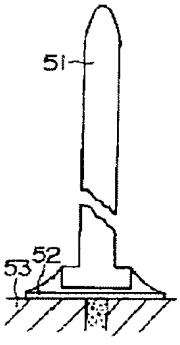

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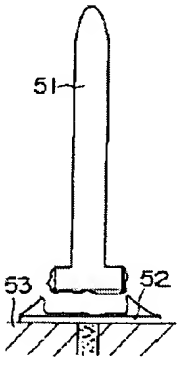

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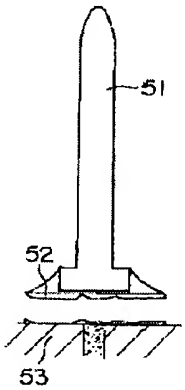

【図１２】